Effect of gate oxidation method on electrical properties of metal-oxide-semiconductor field-effect transistors fabricated on 4H-SiC C(0001) face

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The effect of gate oxidation method on the electrical properties of metal-oxide-semiconductor field-effect transistors (MOSFETs) fabricated on 4H-SiC C(0001) face has been investigated. In the case of SiC MOSFETs fabricated by dry gate oxidation, the peak value of field-effect mobility ($\mu_{FE}$) is 16.3 $\text{cm}^2/\text{V s}$. On the other hand, pyrogenic gate oxidation and pyrogenic gate oxidation followed by $\text{H}_2$ postoxidation annealing (POA) considerably decreased the interface trap density ($D_{it}$) and the threshold voltage, and markedly improved the $\mu_{FE}$. The depth profiles of hydrogen density were measured using secondary ion mass spectroscopy. These verified that pyrogenic gate oxidation increases hydrogen density at the SiO$_2$/SiC interface compared to dry gate oxidation, and that the pyrogenic gate oxidation followed by $\text{H}_2$ POA increases considerably it. It is thought that the $D_{it}$ reduction might be caused by the passivation of interface states by $-\text{H}$ or $-\text{OH}$. The peak value of $\mu_{FE}$ for SiC MOSFETs fabricated by pyrogenic gate oxidation followed by $\text{H}_2$ POA is 111 $\text{cm}^2/\text{V s}$, which is much higher than that of SiC MOSFETs fabricated on a Si(0001) face. Therefore, the 4H-SiC C(0001) face is suitable for the fabrication of SiC power MOSFETs. © 2004 American Institute of Physics. [DOI: 10.1063/1.1682680]

Silicon carbide (SiC) is considered an excellent material for next-generation high-power, high-temperature, and high-frequency devices because it has wide energy gap, high thermal conductivity, and high dielectric field. SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) are investigated for fast switching devices. SiC MOSFETs have been mainly fabricated on the Si(0001) face or the (1120) face. The oxidation ratio of the C(000\bar{1}) face is the largest among all hexagonal SiC faces, which is approximately ten times larger than that of the Si(0001) face. Therefore, the oxidation processes time which require thick oxide films of a few hundred nanometers for the fabrication of SiC MOSFETs can be shortened using the C(000\bar{1}) face. However, there has been no report showing that MOSFETs fabricated on the C(000\bar{1}) face can operate without channel doping using nitrogen under the gate oxide because the operation of inversion type for MOSFETs on the (0001) face was very difficult. We reported that the $D_{it}$ at the shallow level of the MOS capacitor fabricated by pyrogenic gate oxidation and $\text{H}_2$ postoxidation annealing (POA) became almost as low as that of MOS capacitors fabricated on the Si(0001) face by dry gate oxidation and $\text{H}_2$ POA, even if the $D_{it}$ on the (0001) face is much higher than that on the Si(0001) face at the deep level. Recently, some groups reported that the $D_{it}$ at the shallow level affected the inversion channel mobility of SiC MOSFETs. Hence, it was expected that the MOSFETs fabricated on the C(000\bar{1}) face can operate without the channel doping if it is fabricated under the gate oxidation condition in which the $D_{it}$ at the shallow level is low.

In this letter, we have investigated the effects of the gate oxidation method on the $D_{it}$ of n-type MOS capacitors, the threshold voltage ($V_{th}$) and field-effect mobility ($\mu_{FE}$) of MOSFETs fabricated on the 4H-SiC C(0001) face. We have also studied the relationship between hydrogen density at the SiO$_2$/SiC interface and the electrical properties of 4H-SiC MOSFETs in order to clarify the reason why gate oxidation method affects the $D_{it}$ and the $\mu_{FE}$. 8° off-angled n-type 4H-SiC C(000\bar{1}) face epitaxial substrates for MOS capacitors were purchased from Cree Research Inc. In the case of p-type epitaxial substrates for MOSFETs, bulk substrates were purchased from Cree Research Inc. and epitaxial growth was performed by our group. The epitaxial growth technique of the C(0001) face is described in Ref. 13. The effective carrier density ($N_a-N_d$) and ($N_a-N_d$) in the n-type and p-type epitaxial layers were approximately $1 \times 10^{16}$ and $4 \times 10^{15}$ $\text{cm}^{-3}$, respectively. First, the RCA cleaning was carried out. Next, a sacrificial oxide of 10 nm thickness was grown at 1100 °C, and then it was removed with 5% HF solution. Gate oxide films were thermally grown at 1100 °C for 45 min in dry $\text{O}_2$ (dry gate oxidation) or 14 min in $\text{H}_2\text{O}$ atmosphere containing $\text{O}_2$ (pyrogenic gate oxidation). The thickness of the gate oxide films was approximately 50 nm. After gate oxidation, all the samples were annealed in argon for 30 min at 1100 °C, and then gradually cooled in argon. We reported that $\text{H}_2$ POA at high temperature decreased the $D_{it}$ at SiO$_2$/SiC on the Si(0001) and the (1120) faces. Therefore, one of the samples with the gate oxide grown using pyrogenic gate oxidation was annealed in $\text{H}_2$ at 800 °C for 30 min and then gradually cooled in $\text{H}_2$. Aluminum was evaporated on the top of the oxide films and...
on the back of the samples in order to form gate electrodes and ohmic contacts, respectively. In the case of n-channel MOSFETs, the source and drain regions were formed by phosphorus ion implantation at 500 °C with the dose of \(7 \times 10^{15} \text{ cm}^{-2}\). After the implantations, postimplantation annealing was then performed at 1500 °C for 5 min in Ar. Gate oxidation was performed under the same conditions as those for n-type MOS capacitors. Aluminum was evaporated to form electrodes of the gate, source, drain, and substrate. Contact annealing was not performed. The channel length \((L)\) and width \((W)\) of the MOSFETs were 100 and 150 \(\mu\text{m}\), respectively. \(D_{\text{it}}\) estimation was carried out using a K182 system, which consists of a Keithley 5900 \(C-V\) analyzer, a 595 quasi-static \(C-V\) meter, and a 5951 remote input coupler. The drain current \((I_d)\) versus the gate voltage \((V_g)\) characteristics were measured at room temperature using a Hewlett–Packard Semiconductor Parameter Analyzer 4156B. All electrical measurements were carried out in a shielded dark box at room temperature. Secondary ion mass spectroscopy (SIMS) analysis using cesium ions was performed in order to measure the depth profiles of hydrogen density of SiO\(_2\)/SiC structures. The gate oxidation and H\(_2\) POA of the samples used in SIMS analysis were performed under the same conditions as those for the fabrication of MOS capacitors and MOSFETs.

Figures 1 and 2 show the \(D_{\text{it}}\) distributions of n-type MOS capacitors and the \(V_{\text{th}}\) dependence of field-effect mobility \((\mu_{\text{FE}})\) for the n-channel MOSFETs fabricated on the C(0001) face. The values of the \(D_{\text{it}}\) were estimated from Page 15 of Ref. 15:

\[
D_{\text{it}} = \frac{1}{q}\left[\frac{1}{1/C_{q} - 1/C_{\text{ox}}} - \frac{1}{1/C_{\text{h}} - 1/C_{\text{ox}}}\right].
\]

The \(V_{\text{th}}\) dependence of \(\mu_{\text{FE}}\) was estimated from \(I_d - V_g\) characteristics measured at the drain voltage \((V_d) = 0.1\ \text{V}\) using

\[
\mu_{\text{FE}} = \frac{\partial I_d/\partial V_g}{1/(C_{\text{ox}}V_d)(L/W)},
\]

where \(q\) is the electric charge, and \(C_{\text{h}}, C_{q}, C_{\text{ox}}\) are the high-frequency, quasistatic, and oxide capacitance per unit area, respectively. The \(D_{\text{it}}\) at \(E_c - E\) from 0.2 to 0.6 \text{ eV} is shown in Fig. 1. The \(D_{\text{it}}\) is underestimated at \(E_c - E\) below approximately 0.2 and above 0.6 \text{ eV}, because the measurements are performed at room temperature.\(^{16,17}\) The peak values of \(\mu_{\text{FE}}\) and threshold voltages \((V_{\text{th}})\) of the three MOSFETs are also summarized in Table I. The \(V_{\text{th}}\) is defined as the intersection point of the \(V_g\) axis and the tangential line drawn from the point of maximum slope in the \(I_d - V_g\) curve.

The values of \(V_{\text{th}}\) of the MOSFETs fabricated by pyrogenic gate oxidation and pyrogenic gate oxidation followed by \(H_2\) POA are approximately one-fifth and one-sixth that of the MOSFETs fabricated with dry gate oxidation, respectively. The \(V_{\text{th}}\) changes by the fixed charges in the SiO\(_2\) films, the charge from carriers trapped at interface states, etc. Harada et al. reported that the \(V_{\text{th}}\) of SiC MOSFETs is affected by the \(D_{\text{it}}\) in the \(E_c - E\) range from 0.2 to 0.4 \text{ eV}.\(^{18}\) The \(D_{\text{it}}\) in the \(E_c - E\) range from 0.2 to 0.4 \text{ eV} of the n-type MOS capacitor fabricated by pyrogenic gate oxidation and pyrogenic gate oxidation followed by \(H_2\) POA is lower than that of the n-type MOS capacitor fabricated by dry gate oxidation as shown in Fig. 1. Therefore, the \(V_{\text{th}}\) of SiC MOSFETs fabricated by pyrogenic gate oxidation and by pyrogenic gate oxidation followed by \(H_2\) POA is lower than that of SiC MOSFETs fabricated by dry gate oxidation.

The values of \(D_{\text{it}}\) of the sample fabricated by dry gate oxidation is the highest among the three samples in the entire range of \(E_c - E\) from 0.2 to 0.6 \text{ eV}. Pyrogenic gate oxidation reduces the \(D_{\text{it}}\), which is approximately half that at the \(E_c\)

![FIG. 1. Distributions of the \(D_{\text{it}}\) of n-type MOS capacitors fabricated on the 4H-SiC C(0001) face as a function of energy from the conduction-band edge. The \(D_{\text{it}}\) was estimated by high-low method.](image1)

![FIG. 2. \(\mu_{\text{FE}}\) as a function of \(V_g\) for MOSFETs fabricated on the 4H-SiC C(0001) face by dry gate oxidation, pyrogenic gate oxidation, and pyrogenic gate oxidation followed by \(H_2\) POA.](image2)

<table>
<thead>
<tr>
<th>Oxidation method</th>
<th>(V_{\text{th}}) (V)</th>
<th>Peak value of (\mu_{\text{FE}}) (cm(^2)/V s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dry oxidation</td>
<td>8.0</td>
<td>16.3</td>
</tr>
<tr>
<td>Pyrogenic oxidation</td>
<td>1.6</td>
<td>98.7</td>
</tr>
<tr>
<td>Pyrogenic oxidation + (H_2) POA</td>
<td>1.4</td>
<td>111.0</td>
</tr>
</tbody>
</table>

**TABLE I.** \(V_{\text{th}}\) and peak value of \(\mu_{\text{FE}}\) of MOSFETs fabricated on 4H-SiC C(0001) face.
The hydrogen density near the SiO$_2$/SiC interface increases in the following order: the sample fabricated by dry gate oxidation, one by pyrogenic gate oxidation, and one by pyrogenic gate oxidation followed by H$_2$ POA. The $D_{it}$ and the hydrogen density obviously correlate with each other. The $D_{it}$ decreases with increasing hydrogen density. It is considered that the $D_{it}$ might be reduced due to the passivation of interface states using $-H$ or $-OH$, resulting in the $V_{th}$ reduction and the $\mu_{FE}$ improvement.

In conclusion, we have studied the gate oxidation technique in order to improve the channel mobility of MOSFETs fabricated on the (0001) face. Pyrogenic gate oxidation and H$_2$ POA decrease the $D_{it}$ and the $V_{th}$, and markedly improve the $\mu_{FE}$, which becomes 111 cm$^2$/V.s. This is much larger than that of MOSFETs fabricated on the Si(0001) face although it is smaller than the already reported maximum $\mu_{FE}$ of MOSFETs fabricated on the (1120) face.\cite{22} However, the field strength of the (1120) face is approximately 70% that of the Si(0001) face and the C(0001) face, and is disadvantageous for the power devices.\cite{22,23} As a result, the C(0001) face is considered to be suitable for DMOS type power MOSFETs because it has large field-effect mobility and field strength, and highest gate oxidation ratio.

$-E=0.2$ eV for the MOS capacitor fabricated by dry gate oxidation. The values of $D_{it}$ near the $E_c - E=0.2$ eV for the MOS capacitor fabricated by H$_2$ POA is lower than that of the MOS capacitor fabricated by only pyrogenic gate oxidation. The difference of $D_{it}$ near 0.2 eV between MOS capacitors fabricated by dry and pyrogenic gate oxidation is larger than that between MOS capacitors fabricated by pyrogenic and pyrogenic gate oxidation followed by H$_2$ POA. The $D_{it}$ at the shallow level below approximately 0.2 eV strongly affected the inversion channel mobility as pointed out by some researchers.\cite{5,11,12,18} The $D_{it}$ below 0.2 eV is not shown in Fig. 1 because it is underestimated as mentioned earlier. However, qualitatively, the difference of $D_{it}$ below 0.2 eV between MOS capacitors fabricated by dry and pyrogenic gate oxidation is larger than that between MOS capacitors fabricated by pyrogenic and pyrogenic gate oxidation followed by H$_2$ POA like near 0.2 eV. Moreover, the $D_{it}$ of MOS capacitor fabricated by pyrogenic gate oxidation followed by H$_2$ POA at the $E_c - E=0.58$ eV is approximately one-third those of the other MOS capacitors. The hydrogen effects on Si(0001) face have been reported.\cite{19} In the C(0001) face, H$_2$ POA is very effective in $D_{it}$ reduction not only in the shallow level, but also the deep level. These results suggest that pyrogenic gate oxidation or pyrogenic gate oxidation followed by H$_2$ POA improves the $\mu_{FE}$. Especially, pyrogenic gate oxidation is considered to be much effective for improvement of inversion channel mobility. Actually pyrogenic gate oxidation greatly improves the $\mu_{FE}$ compared to the dry gate oxidation, and H$_2$ POA further improves the $\mu_{FE}$ as shown in Fig. 2. Finally, the $\mu_{FE}$ peak value of 111 cm$^2$/V.s is achieved for the MOSFETs fabricated by pyrogenic gate oxidation followed by H$_2$ POA. This value is much higher than that of MOSFETs fabricated on the Si(0001) face.\cite{20} The (001) face is more suitable for the fabrication of power MOSFETs compared to the Si(0001) face.

Figure 3 exhibits the depth profiles of the hydrogen density of the three SiO$_2$/SiC structures measured using SIMS.

![FIG. 3. Depth profiles of hydrogen density for SiO$_2$/SiC structures prepared using dry gate oxidation, pyrogenic gate oxidation, pyrogenic gate oxidation followed by H$_2$ POA.](image-url)